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| EXAMINER | |
|---|---|
| DO, CHAT C | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/823,929 | ORCHARD, JOHN T. | |
| | Examiner | Art Unit | |
| | Chat C. Do | 2193 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *50-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This communication is responsive to Amendment filed 11/02/2007.

2. Claims 50-99 are pending in this application. Claims 50, 70, 85, and 93 are independent claims. In Amendment, claims 1-49 are cancelled and claims 50-99 are added. This Office Action is made final.

### *Claim Rejections - 35 USC § 101*

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 50-99 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 50-99 cite a method and apparatus for performing sum of partial products in accordance with a mathematical algorithm. However, claims 50-99 merely disclose steps/components for performing sum of partial products without further disclosing a practical/physical application and further the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 50-99 are directed to non-statutory subject matter.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 50-56, 58-60, 63-67, 70-76, 78-79, 82-86, 88, 90-97, and 99 are rejected under 35 U.S.C. 102(e) as being anticipated by Grisamore (U.S. 6,535,901).

Re claim 50, Grisamore discloses in Figures 1-9 a system (e.g. general seen in Figure 1 and abstract) comprising:

a plurality of multi-bit inputs (e.g. as first current multiplicand 20 and second current multiplicand 22 wherein each of the multiplicand consists of plurality of bits as seen in Figure 4);

a combinational stage configured to generate a plurality of partial products of the plurality of multi-bit inputs (e.g. partial product generator 12 in Figure 1 wherein the generator consists of a plurality of sub-stages as seen in col. 1 lines 42-47 for generating a corresponding plurality of partial products);

a hybrid summing module comprising one or more full adders, one or more half adders, and a plurality of registers (e.g. reduction tree module 14 and detail of structure operation is seen in Figure 5 wherein the dash-circle of two dots indicates a half adder and the dash-circle of three dots indicates a full adder, other non-circle indicates storing

means by appropriated registers as explained in col. 1 lines 33-42 for synchronizing in pipeline as convention in the art of technology);

where the hybrid summing module is configured to receive as inputs the plurality of partial products (e.g. as the reduction tree module 14 interfaces and receives a plurality of partial products generated from the partial product generator 12 in Figure 1), and is configured to reduce the plurality of partial products (e.g. as clearly label by the reduction tree module 14 in Figure 1) to a first partial summation and a second partial summation via the one or more full adders and the one or more half adders (e.g. Figure 5 wherein stages 3-4 are the reduction operations of the reduction tree module 14 in Figure 1);

where outputs of each of the one or more full adders and outputs of each of the one or more half adders are coupled to inputs of respective ones of the plurality of registers (e.g. as seen in Figure 5 wherein each one of the dot is considered as register); and

where any bits of the plurality of partial products that are not coupled to an input of one of the one or more full adders or to an input of one of the one or more half adders are coupled to inputs of respective ones of the plurality of registers (e.g. as col. 1 lines 33-42 clearly explains a plurality of registers are needed at appropriated points within the reduction module 14 in Figure 1 in order for the pipelining provides a high throughput as conventional design well-known in the art of technology).

Re claim 51, Grisamore further discloses in Figures 1-9 the hybrid summing module further comprises a two-input adder (e.g. adder 18 in Figure 1), the two-input adder configured to receive the first partial summation and the second partial summation

as inputs (e.g. as the first resultant 16 and second resultant 28 in Figure 1 respectively), and configured to produce a final summation (e.g. output of adder 18 as multiplied resultant 34 in Figure 1, note with the feedbacks 26 and 28, the output result would be the multiplied accumulated resultant).

Re claim 52, Grisamore further discloses in Figures 1-9 the hybrid summing module is further configured to receive the final summation (e.g. as the output of the memory 16 in Figure 1 for feeding back the previous results to the current in order to produce the accumulation result), and is further configured to reduce the final summation and the plurality of partial products to a first accumulated partial summation and a second accumulated partial summation via the one or more the adders and the one or more half adders (e.g. Figure 1 and Figure 5).

Re claim 53, Grisamore further discloses in Figures 1-9 bits of the final summation are coupled to inputs of respective ones of the plurality of registers (e.g. as memory 16 in Figure 1).

Re claim 54, Grisamore further discloses in Figures 1-9 the combinational stage and the hybrid summing module are configured to implement a multiply-accumulate operation (e.g. as Figure 1 with the feedback system to implement the multiply-accumulate).

Re claim 55, Grisamore further discloses in Figures 1-9 a summing module generator adapted to configure the hybrid summing module to reduce the plurality of partial products (e.g. as clearly label in the reduction tree module 14 in Figure and also can be seen the reduction operation taking place in Figure 5 with sub-stages 2-4 to take

multiple inputs and output only a final result); and where the combinational stage, the hybrid summing module, and the summing module generator are parts of a single integrated circuit (e.g. Figure 1 and col. 1 lines 10-32 as single integrated circuit).

Re claim 56, Grisamore further discloses in Figures 1-9 the summing module generator comprises one or more control elements (e.g. Figure 9).

Re claim 58, Grisamore further discloses in Figures 1-9 the one or more control elements are configured to implement the summing model generator as an application (e.g. multiply accumulation application as seen in Figure 1).

Re claim 59, Grisamore further discloses in Figures 1-9 the summing model generator is configured to generate the hybrid summing module (e.g. Figure 9).

Re claim 60, Grisamore further discloses in Figures 1-9 the summing model generator is configured to dynamically reallocate resources of the single integrated circuit to implement the hybrid summing module (e.g. Figure 9 and col. 1 lines 10-20 as dynamically and optimally control the resource).

Re claim 63, Grisamore further discloses in Figures 1-9 each of at least some of the LUTs are associated with ones of the plurality of registers (e.g. inherently in view of col. 1 lines 33-42).

Re claim 64, Grisamore further discloses in Figures 1-9 the summing model generator is configured to enable at least some of the resources as the one or more full adders (e.g. Figure 9 by determining and activating a number of full adders 86).

Re claim 65, Grisamore further discloses in Figures 1-9 the summing model generator is configured to enable at least some of the resources as the one or more the

adders, the one or more half adders, and the plurality of registers (e.g. perform by the component 86 in Figure 9 wherein a number of half-adder, full-adder, and registers are needed for the reduction size of the partial products).

Re claim 66, Grisamore further discloses in Figures 1-9 the summing model generator is configured to program an interconnection of the one or more full adders, the one or more half adders, and the plurality of registers to, at least in part, implement the hybrid summing module (e.g. Figure 9).

Re claim 67, Grisamore further discloses in Figures 1-9 the summing model generator is configured to analyze a number of bits of equal significance among the plurality of partial products to determine (e.g. by components 80-84 in Figure 9), at least in part, a number of the one or more full adders, a number of the one or more half adders, and a number of the plurality of registers to implement the hybrid summing module (e.g. by component 86 in Figure 9).

Re claim 70, it has similar limitations cited in claim 50. Thus, claim 70 is also rejected under the same rationale as cited in the rejection of rejected claim 50.

Re claim 71, it has similar limitations cited in claim 51. Thus, claim 71 is also rejected under the same rationale as cited in the rejection of rejected claim 51.

Re claim 72, it has similar limitations cited in claim 52. Thus, claim 72 is also rejected under the same rationale as cited in the rejection of rejected claim 52.

Re claim 73, it has similar limitations cited in claim 53. Thus, claim 73 is also rejected under the same rationale as cited in the rejection of rejected claim 53.

Re claim 74, Grisamore further discloses in Figures 1-9 a combinational stage configured to generate the plurality of addends as partial products of a plurality of multi-bit inputs (e.g. Figures 1 and 5).

Re claim 75, it has similar limitations cited in claim 54. Thus, claim 75 is also rejected under the same rationale as cited in the rejection of rejected claim 54.

Re claim 76, it has similar limitations cited in claim 56. Thus, claim 76 is also rejected under the same rationale as cited in the rejection of rejected claim 56.

Re claim 78, it has similar limitations cited in claim 59. Thus, claim 78 is also rejected under the same rationale as cited in the rejection of rejected claim 59.

Re claim 79, it has similar limitations cited in claim 60. Thus, claim 79 is also rejected under the same rationale as cited in the rejection of rejected claim 60.

Re claim 82, it has similar limitations cited in claim 64. Thus, claim 82 is also rejected under the same rationale as cited in the rejection of rejected claim 64.

Re claim 83, it has similar limitations cited in claim 65. Thus, claim 83 is also rejected under the same rationale as cited in the rejection of rejected claim 65.

Re claim 84, it has similar limitations cited in claim 66. Thus, claim 84 is also rejected under the same rationale as cited in the rejection of rejected claim 66.

Re claim 85, it has similar limitations cited in claim 50. Thus, claim 85 is also rejected under the same rationale as cited in the rejection of rejected claim 50.

Re claim 86, it has similar limitations cited in claim 55. Thus, claim 86 is also rejected under the same rationale as cited in the rejection of rejected claim 55.

Re claim 88, it has similar limitations cited in claim 59. Thus, claim 88 is also rejected under the same rationale as cited in the rejection of rejected claim 59.

Re claim 90, it has similar limitations cited in claim 51. Thus, claim 90 is also rejected under the same rationale as cited in the rejection of rejected claim 51.

Re claim 91, it has similar limitations cited in claim 52. Thus, claim 91 is also rejected under the same rationale as cited in the rejection of rejected claim 52.

Re claim 92, it has similar limitations cited in claim 54. Thus, claim 92 is also rejected under the same rationale as cited in the rejection of rejected claim 54.

Re claim 93, Grisamore discloses in Figures 1-9 method of using an integrated circuit (e.g. Figure 1) comprising: implementing, via a summing module generator of the integrated circuit, a hybrid summing module on the integrated circuit (e.g. by components 14 and 16 in Figure 1); and performing, using the hybrid summing module, a multiply operation (e.g. Figure 1 without the feedback resultants 26 and 28 in Figure 1).

Re claim 94, it has similar limitations cited in claim 51. Thus, claim 94 is also rejected under the same rationale as cited in the rejection of rejected claim 51.

Re claim 95, it has similar limitations cited in claim 52. Thus, claim 95 is also rejected under the same rationale as cited in the rejection of rejected claim 52.

Re claim 96, Grisamore further discloses in Figures 1-9 the implementing further comprises coupling outputs of each of the one or more full adders and outputs of each of the one or more half adders to inputs of respective ones of the plurality of registers (e.g. Figure 5), and coupling any bits of the plurality of addends that are not coupled to an

input of one of the one or more full adders or to an input of one of the one or more half adders to inputs of respective ones of the plurality of registers (e.g. col. 1 lines 33-42).

Re claim 97, Grisamore further discloses in Figures 1-9 the implementing further comprises analyzing a number of bits of equal significance among the plurality of addends to determine, at least in part, a number of the one or more full adders, a number of the one or more half adders, and a number of the plurality of registers to implement the hybrid summing module (e.g. Figure 9).

Re claim 99, it has similar limitations cited in claim 60. Thus, claim 99 is also rejected under the same rationale as cited in the rejection of rejected claim 60.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 57, 61-62, 77, 80-81, 87, 89, and 98 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grisamore (U.S. 6,535,901) in view of Chang et al. ("Hardware-efficient implementations for discrete function transforms using LUT-based FPGAs").

Re claim 57, Grisamore fails to disclose in Figures 1-9 the one or more control elements are Combinational Logic Blocks (CLBs). However, Change et al. disclose the one or more control elements are Combinational Logic Blocks (CLBs) (e.g. introduction section in page 309 left column).

Therefore, it would have been obvious to a person having ordianry skill in the art at the time the invention is made to add the one or more control elements are Combinational Logic Blocks (CLBs) as seen in Chang et al.'s invention into Grisamore's invention because it would enable to efficient implementing a configurable logic function (e.g. page 309 abstract and section 1 introduction).

Re claim 61, Grisamore fails to disclose in Figures 1-9 the single integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and where the resources comprise at least some of the CLBs. However, Chang et al. disclose the single integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and where the resources comprise at least some of the CLBs (e.g. abstract, section I introduction in page 309 and section 3.3 hardware cost analysis).

Therefore, it would have been obvious to a person having ordianry skill in the art at time the invention is made to add the single integrated circuit is a Field Programmable Gate Array (FPGA), the FPGA comprises a plurality of Combinational Logic Blocks (CLBs); and where the resources comprise at least some of the CLBs as seen in Chang et al.'s invention into Grisamore's invention because it would enable to reduce the hardware cost for performing logic functions (e.g. second paragraph on the left column page 309).

Re claim 62, Grisamore fails to disclose in Figures 1-9 the single integrated circuit comprises a plurality of Boolean function generators, the Boolean function generators comprising look-up tables (LUTs) to implement Boolean logic functions; and where the resources comprise at least some of the plurality of Boolean function

generators. However, Chang et al. disclose the single integrated circuit comprises a plurality of Boolean function generators, the Boolean function generators comprising look-up tables (LUTs) to implement Boolean logic functions; and where the resources comprise at least some of the plurality of Boolean function generators (e.g. left column page 310 lines 1-5).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the single integrated circuit comprises a plurality of Boolean function generators, the Boolean function generators comprising look-up tables (LUTs) to implement Boolean logic functions; and where the resources comprise at least some of the plurality of Boolean function generators as seen in Chang et al.'s invention into Grisamore's invention because it would enable to reduce the hardware cost (e.g. introduction section on page 309 lines 7-15).

Re claim 77, it has similar limitations cited in claim 57. Thus, claim 77 is also rejected under the same rationale as cited in the rejection of rejected claim 57.

Re claim 80, it has similar limitations cited in claim 61. Thus, claim 80 is also rejected under the same rationale as cited in the rejection of rejected claim 61.

Re claim 81, it has similar limitations cited in claim 62. Thus, claim 81 is also rejected under the same rationale as cited in the rejection of rejected claim 62.

Re claim 87, it has similar limitations cited in claim 61. Thus, claim 87 is also rejected under the same rationale as cited in the rejection of rejected claim 61.

Re claim 89, it has similar limitations cited in claim 61. Thus, claim 89 is also rejected under the same rationale as cited in the rejection of rejected claim 61.

Re claim 98, it has similar limitations cited in claim 61. Thus, claim 98 is also rejected under the same rationale as cited in the rejection of rejected claim 61.

9. Claims 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grisamore (U.S. 6,535,901) in view of Eric ("Complex Multiplication").

Re claims 68-69, Grisamore fails to disclose in Figures 1-9 a negater; and where at least some of the plurality of partial products are configured to pass through the negater prior to being received as inputs of the hybrid summing module and the combinational stage, the negater, and the hybrid summing module are configured to implement a real portion of a complex multiply operation. However, Eric discloses in page 1 of article "Complex Multiplication" the negater (e.g. as for inverting the partial term bd in expression 2); and where at least some of the plurality of partial products are configured to pass through the negater (e.g. as term ac does not need to invert in expression 2) prior to being received as inputs of the hybrid summing module and the combinational stage, the negater, and the hybrid summing module are configured to implement a real portion of a complex multiply operation (e.g. the sum term in expression 2 without imaginary part).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a negater; and where at least some of the plurality of partial products are configured to pass through the negater prior to being received as inputs of the hybrid summing module and the combinational stage, the negater, and the hybrid summing module are configured to implement a real portion of a complex

multiply operation as seen in Eric's teaching into Grisamore's invention because it would enable to yield a correct result for complex multiplication (e.g. page 1 of Eric article).

### *Response to Arguments*

10. Applicant's arguments with respect to claims 50-99 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

December 15, 2007